



# UltraSPARC-IV Errata

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## 1. Errata Table

**Table 1: UltraSPARC IV Errata**

<b>Errata #</b>	<b>Version 2.3</b>	<b>Version 2.4</b>	<b>Version 3.1</b>	<b>Version 3.2</b>	<b>See ...</b>
1	✓	✓	✓	✓	page 4
2	✓	✓	✓	✓	page 4
3	✓	✓	✓	✓	page 5
4	✓	✓	✓	✓	page 6
5	✓	✓	✓	Not applicable	page 6
6	✓	Not applicable	Not applicable	Not applicable	page 7
7	✓	✓	✓	✓	page 8



## **2. Errata Descriptions and Workarounds**

**Erratum #1: When the outgoing transaction buffer is full, a pending outgoing interrupt request causes data contention with a foreign system bus write of IO for store (WIO).**

**Applicability:**

UltraSPARC IV versions 2.3, 2.4, 3.1, and 3.2.

**Description:**

When the outgoing transaction buffer in the Transaction Out Buffer (TOB) is full, it cannot accept an outgoing interrupt. If the Coherent Pending Queue (CPQ) is processing a foreign system bus write of IO for store (WIO) write to one of the Memory Controller Unit (MCU) control registers at the same time, a data contention occurs in the mux that selects the Address Space Identifier (ASI) write data and the foreign WIO data.

**Impact:**

This data contention causes incorrect data to be written into the MCU control registers.

**Workaround:**

Issue a foreign WIO request only when the processor is in a quiescent state without any outstanding outgoing requests.

**Status:**

This bug will not be fixed in future releases of the silicon.

**Erratum #2: Two CPUs without explicit synchronization doing instruction modification may cause both CPUs to hang and corrupt data.**

**Applicability:**

UltraSPARC IV versions 2.3, 2.4, 3.1, and 3.2.

**Description:**

CPU (CPU "A") executes a load instruction that cannot be serviced by the on-chip data cache while another CPU (CPU "B") modifies CPU A's load instruction during a window of time that spans the initial fetching of the load instruction and a subsequent refetching of that same load instruction.

**Impact:**

The two CPUs may deadlock and depending on how CPU B modifies CPU A's load instruction, data corruption may also occur (this situation will not occur in the case of a single CPU that is executing self-modifying code).

**Workaround:**

Do not modify code running on another CPU without explicit synchronization. If an instruction must be modified without synchronization, avoid using all types of load instructions.

**Status:**

This bug will not be fixed in future releases of the silicon.

**Erratum #3: Privileged mode store alternate using Address Space Identifier (ASI) 0x64 hangs the machine.****Applicability:**

UltraSPARC IV versions 2.3, 2.4, 3.1, and 3.2.

**Description:**

In privileged mode, a store alternate operation using Address Space Identifier (ASI) 0x64 should be flagged as using an illegal ASI and should result in a `data_access_exception` trap. But this checking is not present, so the store is allowed to execute and is never acknowledged.

**Impact:**

The machine hangs in privileged mode (behavior in user mode is correct, so a malevolent user cannot hang the machine).

**Workaround:**

The privileged code should not issue store alternates to ASI 0x64.

**Status:**

This bug will not be fixed in future releases of the silicon.

**Erratum #4: The Floating Point Disabled (FP\_Disabled) Trap is taken with the PDIST instruction when DCR.IFPOE is disabled.****Applicability:**

UltraSPARC IV versions 2.3, 2.4, 3.1, and 3.2.

**Description:**

The processor sometimes takes an Floating Point Disabled (FP\_Disabled) trap when the floating-point unit is enabled (PSTATE.PEF == 1 and FPRS.FEF == 1) and the Interrupt Floating-Point Operation Enable mode bit is disabled (DCR.IFPOE == 0).

**Impact:**

The processor may generate an FP\_Disabled trap when IFPOE = 0. This bug only affects Pixel Component Distance (PDIST) instructions that trigger recirculations.

**Workaround:**

There is no workaround to bypass this problem.

**Status:**

This bug will not be fixed in future releases of the silicon.

**Erratum #5: The protocol error on the system bus (PERR) is reported from programs that have heavy write transactions.****Applicability:**

UltraSPARC IV versions 2.3, 2.4, and 3.1.

**Description:**

The effect of a canceled writeback (WB) stops the memory write transaction of a prior write request to the same memory bank. This causes the TargId that's being used by the prior write to be unable to retire and all the subsequent requests to the same memory bank cannot be dequeued from the memory request queue.

- The two write transactions that affect each other need to come from the same CPU with the same transaction ID and also target to the same CPU memory bank.
- The write transaction to the target CPU needs to be heavy enough to use up all regular TargId.

**Impact:**

Many types of PERR (i.e., a protocol error has occurred on the system bus) timeout errors (e.g., Coherent Pending Queue [CPQ\_TO], TargId [TID\_TO], and Write Queue [WQ\_TO]) falsely assert the ERROR pin.

**Workaround:**

There is no workaround to bypass this problem.

**Status:**

This bug will not be fixed in future releases of the silicon.

**Erratum #6: The internal processor error (IERR) is reported from programs with heavy write transactions targeting one CPU.****Applicability:**

UltraSPARC IV version 2.3.

**Description:**

Once the Memory Controller Unit (MCU) receives the write data ready for a zero targId case, it can start another write data check for the next entry that might again use a zero targId. When there are heavy write transactions targeting one CPU, however, the control logic does not process all of the control signals in time. When this happens, a spurious wrt\_data\_ready will be sent to the MCU bank, which causes the MCU to send a wrt\_data\_request prematurely.

**Impact:**

Many types of internal processor errors (IERRs) (e.g., unexpected write data request [WRD\_UE], Undefined DTransID [UDT], or overwrite a valid S2M RAM entry [S2M\_WER]) falsely assert the ERROR pin.

**Workaround:**

There is no workaround to bypass this problem.

**Status:**

This bug will not be fixed in future releases of the silicon.

**Erratum #7: An incorrect context number is placed in the Data Memory Management Unit (DMMU) Tag Access register after a data\_access\_exception trap.****Applicability:**

UltraSPARC IV versions 2.3, 2.4, 3.1, and 3.2.

**Description:**

When a floating point load on the AX pipe takes a data\_access\_exception trap, the wrong context number may be saved in the context field of the Data Memory Management Unit (DMMU) Tag Access register (ASI 0x58, VA=0x30).

**Impact:**

The incorrect context number is provided to the data\_access\_exception trap handler.

**Workaround:**

Use the CT field (context ID) of the DMMU Synchronous Fault Status register (SFSR, ASI 0x58, VA=0x18). The data\_access\_exception trap handler should refer to either the primary, secondary, or nucleus context registers to convert the 2-bit context ID into a 13-bit context number. See the bug tool for a code snippet.

**Status:**

This bug will not be fixed in future releases of the silicon.